A HIGH-PERFORMANCE INTEGRATED TRUE GRAPHIC PROCESSOR

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Abstract

The first soon available true graphic display processor (G.D.P.) will be presented. It displays an up to 512 x 512 portion of a 4 096 x 4 096 pixel image. Vector drawing speed reaches 560 ns/pixel and 96 variable size and orientation characters are available.

Summary

When a graphic terminal is made with a raster scan video monitor, current image status should be present in a screen refresh memory. If speed of image building is not of prime interest, this memory is mapped into the adressing field of a microprocessor, which prepares or modifies image coding in time - sharing with display automata. As every pixel must be computed by appropriate routines, the moving object "complexity x speed" product is severely limited. To overcome this limitation, image should be described in terms of more complex items at the processor level, symbols or vectors for example.

Thanks to MOS LSI technology, the dedicated automata needed to translate these items into strings of refresh memory bits may be designed as an intelligent peripheral, such as the G.D.P., able to work as a coprocessor of any 8 bit microprocessor.

The architecture of a graphic terminal made with the G.D.P., shown in fig 1 looks no more complex than most sophisticated alphanumeric ones. Note that the image memory is not mapped into the microprocessor addressing field, leaving all the space for the program, and that a complete asynchronism between the display clock and the master processor clock is achieved.

The G.D.P. is seen from the master as a bank of 12 registers : instruction register and status register are located at the same address (the first in write only, the other read only). Two read only registers are used to record light pen coordinates. The eight others are read/write registers and are used to keep the record of G.D.P. working mode and current operations. Dialog between master and G.D.P. is made on a ready/busy bases. The completion of principal commands generates several types of interrupt

signals which can be separately masked at the G.D.P. level.

Vector Generator : A dedicated hardware has been designed which implements the BRESENHAM algorithm (1) with the help of counters, multiplexer and adders. Special care has been taken to minimize the number N of necessary clock cycles to draw a vector. Assuming m = Greatest ($|\Delta X|$, $|\Delta Y|$), then N = m + 3, leading to a drawing speed of 560 ns/pixel. As access to the memory is normally not allowed during display time the mean value of drawing speed is 1.36 µs/pixel (700 µs to draw a full screen diagonal). Extra hardware is used to allow one full line and three types of interrupted lines.

Symbol generator : 96 different symbols may be drawn into the refresh memory from an internal ROM recording the shapes in a 5 x 8 dot matrix. These symbols may be separately X or/and Y scaled up to 16 times, normal or flipped, and horizontally or vertically drawn. The standard ROM is ASCII coded.

Programming the G.D.P. is done by periodically (when necessary !) updating the internal registers and delivering to the instruction register the proper 8 bit opcode. Among the 256 possible opcodes, 128 (with MSB = 1) are used for small vector ($|\Delta X|$ or $|\Delta Y| \leqslant 3$) to maximise curviline drawing speed. The 128 others may be considered as 7 bit ASCII codes, where 96 (column 2 to 7) are shape codes (96 alphanum characters), and 32 are command codes : 16 codes are used for vector drawing, 16 are special functions.

The G.D.P. allows the implementation of high performance graphic terminals with fast moving complex objects capability. The number of colours is only limited by the amount of external memory.

References :

(1) J.E. BRESENHAM "Algorithm for Computer of a digital Platter"
IBM System J - 4 1965 p. 25 - 30

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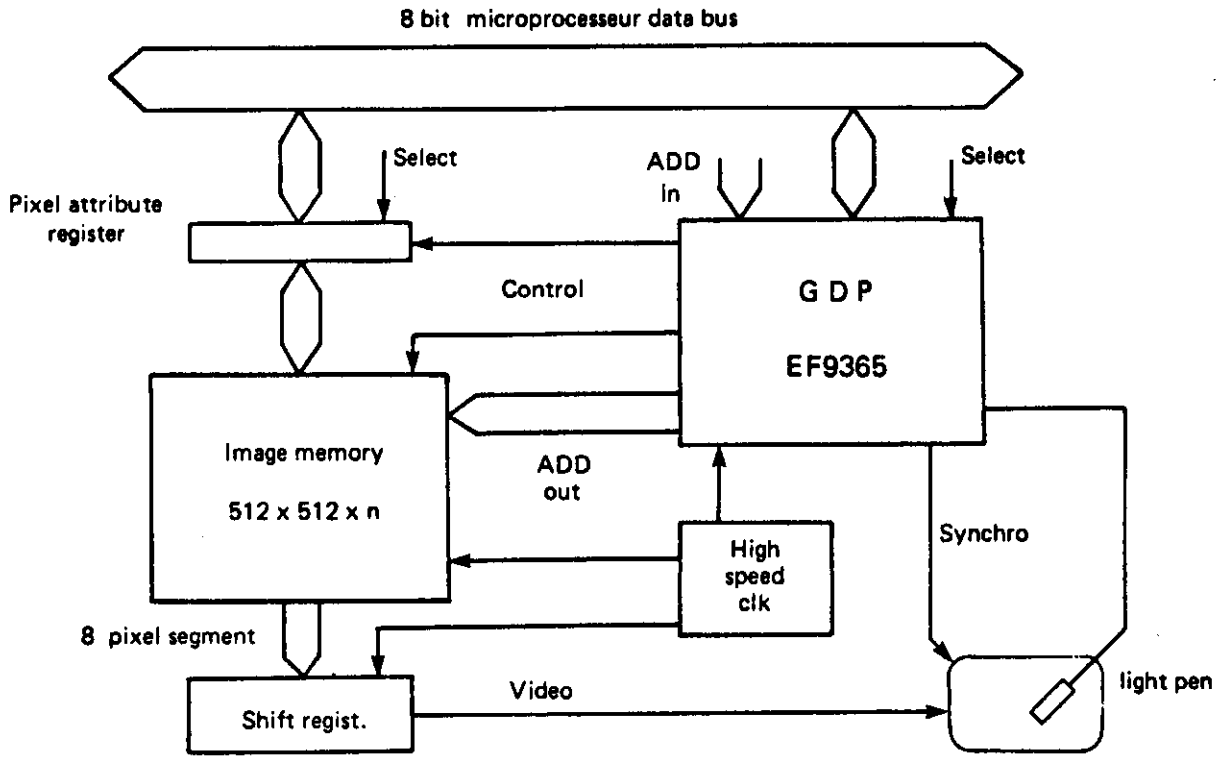

FIGURE 1 – TYPICAL APPLICATION BLOCKDIAGRAM

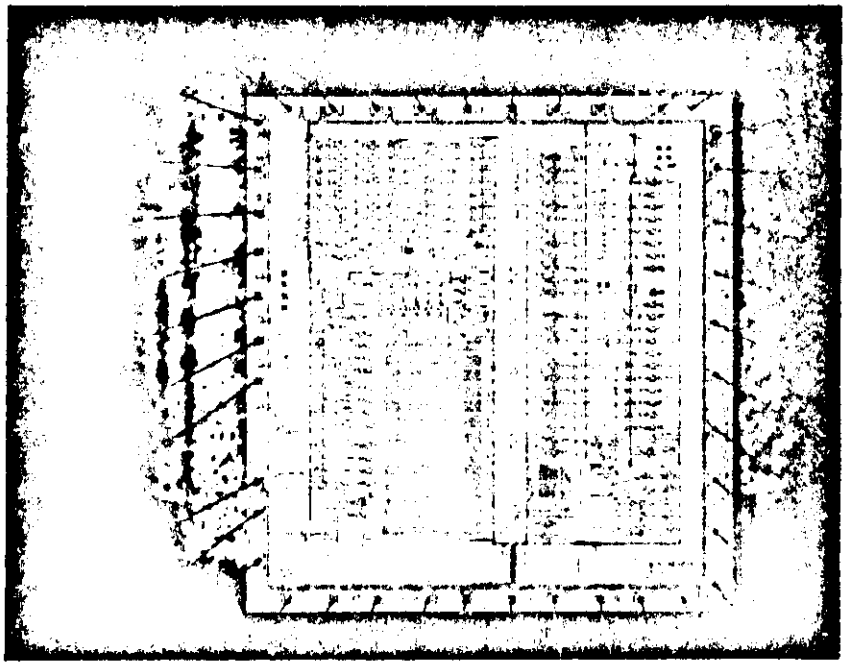

FIGURE 2 – THE GDP "EF9365" IS MADE WITH N CHANNEL SILICON GATE MOS TECHNOLOGY